REMARKS

Applicants hereby traverse the outstanding rejections and request reconsideration and withdrawal in view of the remarks contained herein. In response to the restriction requirement, Applicants have elected, with traverse, examination of Claims 18-29, and the Examiner has withdrawn Claims 11-17 from further consideration. Claims 18-29 are pending in this application.

Applicant's Record Under § 713.04 of Telephone Interview With Examiner

Applicant's attorney thanks the Examiner for his time and consideration in the Examiner-initiated telephone interview of September 28, 2004. Applicant respectfully submits the following record of that telephone interview, under M.P.E.P. § 713.04.

The following persons participated in the interview: Examiner Joseph D. Torres and Applicant's attorney Michael Papalas. The restriction requirement was discussed and a provisional election was made with traverse to prosecute the invention of Claims 18-29.

Restriction Requirement

In response to the Examiner's restriction requirement in which the Applicants provisionally elected group II, with traverse, in the telephone interview of September 28, 2004, Applicants hereby affirm the election group II, which includes claims 18-29 as defined by the restriction requirement, for further prosecution. The election is being made WITH TRAVERSE. Applicants respectfully request reconsideration and withdrawal of the restriction requirement in light of the arguments set forth below.

Restriction is proper if two criteria are satisfied, namely that the inventions are independent or distinct, and that there is a serious burden on the examiner, see M.P.E.P. § 803.

It is well settled that for inventions to be properly restricted, there must be a serious burden on the examiner if restriction is not required, see, M.P.E.P. § 803. The invention of group I has already been searched by virtue of the Examiner's prior art rejection. (see the Office Action dated June 4, 2004) The invention of group II has also been searched, both in

the Office Action dated June 4, 2004, where the Examiner made a prior art rejection of Claims 18-20, and in the present Office Action where the Examiner has made an additional prior art rejection of the claims of group II, namely Claims 18-29. Thus, any search required for the present claims of group I is presumed to have been performed in the search for the claims as they existed for the Office Action of June 4, 2004. As a search has already been completed for both groups identified by the Examiner, there is no serious burden on the Examiner to examine the entire application on the merits, thereby making a restriction improper under MPEP § 803. Specifically, Applicants note that all references cited by the Examiner in the pending Office Action appeared on the search report in the June 4, 2004 Office Action which included the search for the claims set forth in group I.

Applicants also believe that the overlap of cited references found in the two Office Actions in the present case, would be expected in any reasonable search by the Examiner, as both groups I and II have common limitations, such as evaluating elements in row-first order, identifying faulty ones of said elements, and generating a count of said identified faulty elements.

Furthermore, the Examiner has mischaracterized the Applicants' invention in the requirement for restriction. Specifically, the Examiner has stated that Group I can be used for "self-testing, comprising a means for evaluating elements", and Group II can be used "in a self-repair system, comprising a means for evaluating elements". Such limitations do not appear in the claims of Group I or Group II, respectively, and are therefore inappropriate mischaracterizations of the claims of Group I and Group II by the Examiner.

Therefore, for the reasons cited above, Applicants believe that restriction between groups I and II is improper. Applicants respectfully request that the Examiner call the below listed attorney if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Rejection under 35 U.S.C. § 103

Claims 18, 19, and 21-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,939,694 to Eaton et al. (hereinafter, "Eaton") in view of U.S. Patent No. 4,460,997 to Harns (hereinafter, "Harns").

To establish a *prima facie* case of obviousness, three basic criteria must be met, see M.P.E.P. § 2143. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Without conceding the second criteria, Applicant respectfully asserts that the combination of references lack all of the claim limitations and that there is no proper motivation to combine the referenced teachings.

Claim 18 defines a method that includes determining a number of said identified faulty ones of said evaluated elements in each plurality of subsets of said memory segments and physically re-mapping said memory segment in response to said declared failure condition. Eaton discloses a memory system that is operable to logically remap defective memory locations to replacement memory locations using substitute memory table 3-11. (column 5, lines 16-19). The substitute memory table of Eaton can either be a look-up table for all memory locations, or a content addressable memory to look up only replaced memory locations. (column 5, lines 20-40 and column 7, lines 21-28). In either case, Eaton's only disclosed means of replacing defective memory locations requires a mapping function in some type of memory, meaning that Eaton logically remaps defective memory cells, in contrast to the physical remapping of Claim 18.

As Eaton only discloses logically remapping defective memory locations, and not the physical remapping set forth in Claim 18, Eaton does not teach or suggest all the claim limitations found in Claims 18. Harns is not relied upon in the Office Action as teaching these limitations. Therefore, Applicants respectfully assert that for the above reasons Claim 18 is patentable over the rejection of record.

Claims 19 and 20 depend from base Claim 18, and thus inherit all limitations of Claim 18. Each of Claims 19 and 20 sets forth features and limitations not recited by the combination of Eaton and Harns. Therefore, Applicants respectfully assert that, for the above reasons, Claims 19 and 20 are patentable over the rejection of record.

Claim 21 requires successively scanning each of a plurality of subsets of said memory segment, wherein each said subsets comprises at least two linear arrays of elements. Claim 21 specifically states that each subset comprises at least two linear arrays of memory elements. The Office Action relies solely upon Eaton as discloses testing individual memory cells 3-5 on memory chips 3-1. (column 4, lines 41-47). Eaton replaces defective individual memory cells, when located, by logically remapping the addresses for the defective cells to replacement cells. (column 5, lines 8-19). Eaton does not disclose a plurality of subsets of said memory segment wherein each subset comprises at least two linear arrays of elements. The Examiner has opined that the 64 byte data records used by Eaton in his error correction code engine 3-3 corresponds to the subsets of the Claim 21. Applicants respectfully assert that this is clearly in error. The error correction code engine of Eaton is a data integrity mechanism between the memory system and the data bus that provides data error checking when data is read from the memory. This data error checking mechanism corrects for bit errors in the 64 bytes before the data is placed on the bus. The data errors checked for by the error correction engine is distinct from the testing and replacement of defective memory cells 3-5 and corrects errors that can occur by means other than defective memory. (column 5, line 61-column 6, line 16). The subsets of Claim 21 are subsets of memory elements and are successively scanned in evaluating the of the memory segment itself. Further, Eaton does not disclose that the records associated with his error correction code engine are made up of at least two linear arrays of elements. Thus Eaton in combination with Harns does not teach all of the limitations of the invention claimed in Claim 21. Therefore, Applicants respectfully assert that for the above reasons Claim 21 is patentable over the rejection of record.

Claims 22-29 depend from base Claim 21, and thus inherit all limitations of Claim 21. Each of Claims 22-29 sets forth features and limitations not recited by the combination of Eaton and Harns. Therefore, Applicants respectfully assert that for the above reasons Claims 22-29 are patent over the rejection of record.

Further, in there is no motivation in Eaton or Harns to combine the means for reading data out of memory described in Harns with the memory system of Eaton. The Examiner has stated that one skilled in the art would be highly motivated to combine Eaton with Harns to provide a means for reading data out of memory in Eaton, and that it would have been obvious to modify Eaton with the teachings of Harns by including use of evaluating elements in row-fast order. Applicant respectfully asserts that the statements of the Examiner are merely conclusory statements of the results of the combination put forward by the Examiner. The statements do not offer any motivation or reasons that the means of reading memory in Harns would have been of any benefit to the memory system of Eaton.

The Examiner continues by stating that the proposed modification would have been obvious because one of ordinary skill in the art would have recognized that evaluating elements in row fast order would have provided the means for reading data out of memory. The conclusion of the Examiner forms a circular argument with respect to the conclusory statements made previously. The Examiner is arguing that one would be motivated to combine Eaton and Harns to provide a means for reading the memory of Harns, and that the modification would be obvious because it would have provided a means for reading the memory of Eaton.

In addition, Eaton already has a means for reading the memory being tested (column 4, lines 48-57), there is no suggestion that a different means for reading the memory would be beneficial, and the Examiner has provided no reasoning, other that conclusory statements, that would show any benefit from using the means of reading memory in Harns with the memory system of Eaton.

It is well settled that the fact that references can be combined or modified is not sufficient to establish a prima facie case of obviousness, M.P.E.P. § 2143.01. As stated above, the language of the recited motivation is circular in nature, stating that it is obvious to make the modification because the achieved result is obvious. In addition, the language used by the Examiner is also conclusory, merely a statement that the reference can be modified, and does not state any desirability for making the modification, nor does the Examiner explain why one would add the means for reading the memory of Harns to Eaton as the

addition would be duplicative to the existing means for reading memory used by Eaton. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990), as cited in M.P.E.P. § 2143.01. Thus, the motivation provided by the Examiner is improper, as the motivation must establish the desirability for making the modification.

For the reasons described above, the Examiner's combination of Eaton with Harns is improper because there is no motivation in either reference to make the combination. As a result, Applicants respectfully request that the Examiner withdraw the rejections based on the combination of Eaton and Harns.

Conclusion

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 10004546-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service Express Mail Label EV482736625US, in an envelope addressed to: MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: 12-06-2004

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